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Kurzanleitung zur Generierung des Zustandsgraphen aus einer Verilog HDL Beschreibung

I. Zustandsautomaten eingeben

```
module statemachine (clk, in, reset, out);
  input   clk, in, reset;
  output  [1:0]out;

  reg     [1:0]out;
  reg     [1:0]state;

  parameter S0 = 0, S1 = 1, S2 = 2;

  always @ (state) begin
    case (state)
      S0:
        out = 2'b01;
      S1:
        out = 2'b10;
      S2:
        out = 2'b11;
      default:
        out = 2'b00;
      endcase
  end

  always @ (posedge clk or posedge reset) begin
    if (reset)
      state <= S0;
    else
      case (state)
        S0:
          state <= S1;
        S1:
          if (in)
            state <= S2;
          else
            state <= S1;
        S2:
          if (in)
            state <= S0;
          else
            state <= S1;
      endcase
  end
endmodule
```

II. Aufruf des RTL Viewers (Tools)

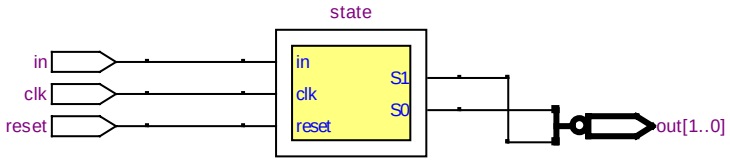
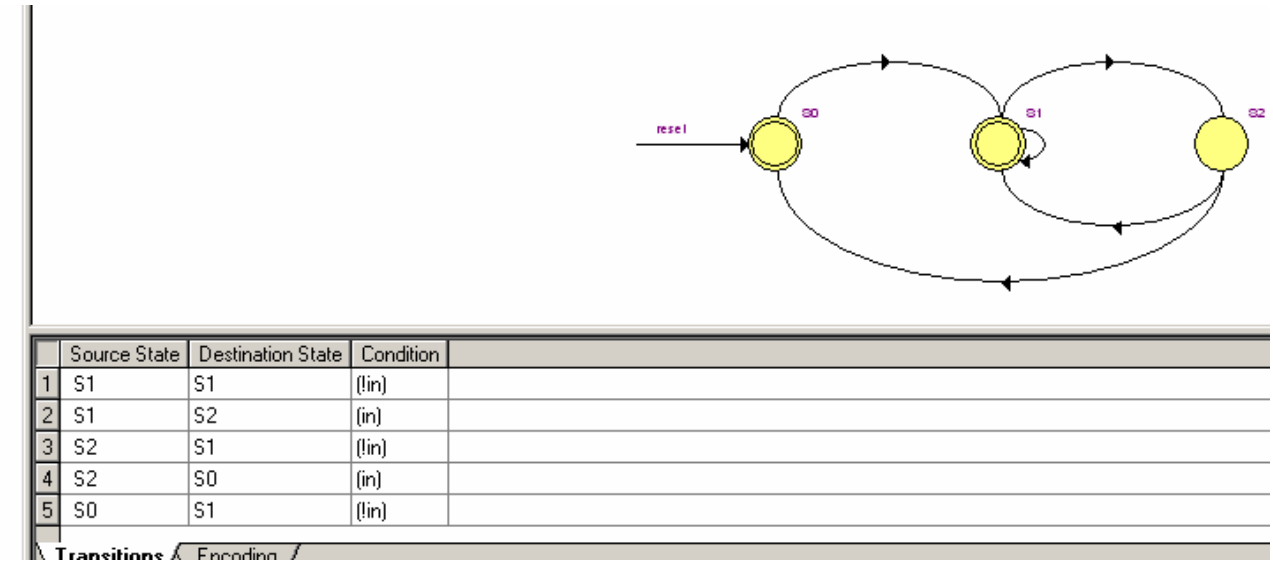


Abbildung 1

III. Doppelclick auf *state* ergibt Abbildung 2.



	Source State	Destination State	Condition
1	S1	S1	(!in)
2	S1	S2	(in)
3	S2	S1	(!in)
4	S2	S0	(in)
5	S0	S1	(!in)

Transitions / Encoding /

Abbildung 2